**BPDC, Dubai - First Semester, 2021-2022**

**DEPARTMENT OF CS**

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| **Course No: CS F342**  **Date: Week #10**  **Id No:** | **TUTORIAL 10** | **Course Title: Computer Architecture**  **Name:** |

1. **cc1 cc2 cc3 cc4 cc5 cc6 cc7 cc8 cc9 cc10**

**L\_1 lw $t2, 60($t1) IF ID Ex MEM WB**

**L\_2 lw $t1, 40($t2) Stall IF ID EX MEM WB**

**L\_3 slt $t1, $t1, $t2 Stall IF ID EX MEM WB**

**L\_4 sw $t1, 20($t2) IF ID EX MEM WB**

**CPI = \_10\_\_ cycles / \_4\_\_ instructions = \_\_2.5 cycles per instruction\_\_\_**

2. Consider an instruction pipeline with four stages with the stage delays 5nsec, 6 nsec, 11 nsec, and 8 nsec respectively. The delay of an inter-stage register stage of the pipeline is 1 nsec. What is the approximate speedup of the pipeline in the steady state under ideal conditions as compared to the corresponding non-pipelined implementation?

Time taken to execute N instructions in non-pipelined implementation will

be (5 + 6 + 11 + 8)N = 30N

Clock period for pipelined implementation = max{5,6,11,8} + 1 = 12.

Time taken for the pipelined implementation = (3 + N)12 = 12N (approx.)

1. Speedup = 30N / 12N = 2.5

3. Minimum clock period = max{5,7,10,8,6} + 1 = 11

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|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| I1 | IF | ID | OF | EX | OW |  |  |  |  |  |  |  |  |  |  |
| I2 |  | IF | ID | OF | EX | OW |  |  |  |  |  |  |  |  |  |
| I3 |  |  | IF | ID | OF | EX | OW |  |  |  |  |  |  |  |  |
| I4 |  |  |  | IF | ID | OF | EX | OW |  |  |  |  |  |  |  |
| I5 |  |  |  |  | .. | .. | .. | .. |  |  |  |  |  |  |  |
| I6 |  |  |  |  | .. | .. | .. | .. |  |  |  |  |  |  |  |
| I7 |  |  |  |  | .. | .. | .. | .. |  |  |  |  |  |  |  |
| I8 |  |  |  |  | .. | .. | .. | .. |  |  |  |  |  |  |  |
| I9 |  |  |  |  |  |  |  | IF | ID | OF | EX | OW |  |  |  |
| I10 |  |  |  |  |  |  |  |  | IF | ID | OF | EX | OW |  |  |
| I11 |  |  |  |  |  |  |  |  |  | IF | ID | OF | EX | OW |  |
| 12 |  |  |  |  |  |  |  |  |  |  | IF | ID | OF | EX | OW |

Total 15 clock cycles are needed, i.e. 14 x 11 = 165 nsec.